REMARKS

Claims 1, 2, 10, 18, and 45 are argued in the Office Action. Claim 1 is independent. Claims 1-54 are currently pending in this application.

Claim Rejection – 35 U.S.C. § 102

Claims 1, 2, 10, 18, and 45 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,619,169 (Matsuura). Applicant respectfully traverses this rejection.

Argued embodiments of the present invention are directed to incorporation of a MOS transistor as the amplifying transistor in a variable gain amplifier, and in particular, a variable gain amplifier that compensates for a decrease in gain (see page 4, first full paragraph; the paragraph bridging pages 4 and 5; first full paragraph of page 5; and first full paragraph in the "Summary of the Invention").

In a variable gain amplifier having a MOS transistor of fixed size (W/L), voltage of the transistor (Vod) remains fixed (at constant current I) when a variable resistor is varied to reduce gain. The current through a MOS transistor is given by

$I = K * (W/L) * Vod^2$ (equation (1), page 4).

Thus, in order to provide a variable gain amplifier with small mount area, for example, by eliminating a variable resistor(s), embodiments of the present invention adjust the size (W/L) of the amplifying transistor.

The variable gain amplifier of the present invention can be used for broadband wireless communication devices. For MOS transistors used in RF transmission, there is a third-order

Input Intercept Point (IIP3) that is an index of a third-order distortion component. The IIP3 of a MOS transistor used in RF transmission is based on the value of Vod.

In the present invention, the size of the amplifying transistor is adjusted by a current path control section. Given the adjustable size (W/L), the voltage Vod which determines the IIP3 of the MOS transistor is given by

$$Vod = \{ I/ (K*W/L)\}^{1/2}$$

Transconductance gm which determines the gain of the transistor can be determined by differentiating the current through the transistor as follows

$$gm = 2 * \{ I * K * W/L\}^{1/2}$$

Based on these relationships, when the size W/L of the transistor is decreased by the current control circuit under current I held at a constant value, the voltage Vod is increased, and the transconductance gm is decreased. When the size W/L of the transistor is increased, the voltage Vod is decreased and the transconductance gm is increased. By making the size of the transistor smaller or larger under constant current flowing through the amplifying transistor, the variable gain amplifier increases or decreases the IIP3 (Specification: page 13).

In summary, the variable gain amplifier of the present invention is arranged such that when the size of the amplifying transistor is decreased or increased under constant current maintained by a current path control section, the IIP3 is increased or decreased and the gain is decreased or increased. Further, with a current control transistor (e.g. 12, Figure 2) in the current path control, the current path through the amplifying transistor can be independently controlled (Specification: page 14, line 21, to page 15, line 13).

The present invention, in disclosed embodiments, relates to operating principles of MOS transistors in an arrangement for a variable gain amplifier without a variable resistor.

Claim 1 is directed to a variable gain amplifier having an amplifying transistor which amplifies an input signal and a current path control section which adjusts a percentage of the amplifying transistor that contributes to amplification of the input signal and adjusts a path of a current through the amplifying transistor.

The Office Action states that Matsuura's transistors 2a and 2b teach the claimed amplifying transistor, and that Matsuura's constant current sources 4a and 4b, and amplitude control circuit teach the claimed current path control section.

Matsuura is directed to a variable gain differential amplifier. A preferred embodiment comprises two pairs of transistors and independent control of two current sources to generate a desired output amplitude. The current sources are used to increase the current values necessary for the two circuits connected in parallel with each other (col. 3, lines 20-23). Matsuura teaches load resistors 3 and 3' and an associated power source in order to obtain respective voltage outputs. Furthermore, the transistors in Matsuura are bipolar.

In particular, Voltages applied to gates of the bipolar transistors through input terminals take on one of two values, H or L. By controlling current value provided at current sources, the output voltage at an associated output terminal can be varied. Variable gain is accomplished through control of the amount of current. The value at an output terminal is $V_{cc} - R_c \times I_E$, where the power source voltage and load resistance are constant. The input logic signal H/L at an input

terminal serves to turn ON or OFF a transistor. Thus, the bipolar transistors do not amplify the input voltages provided at input terminals.

Because the bipolar transistors do not amplify the input voltages, Matsuura does not teach the claimed "amplifying transistor" which amplifies an input signal and the "current path control section" which adjusts a percentage of the amplifying transistor that contributes to "amplification of the input signal." Thus, Applicant submits that Matsuura fails to teach each and every claimed element of claim 1.

Furthermore, with respect to claim 45, unlike the present invention, Matsuura discloses varying the range of output amplitude by varying the current value (e.g., as shown in Figs. 2 and 3). The current path control section of claim 45 varies the percentage of the amplifying transistor, and controls and maintains a current flow through the amplifying transistor at a constant level. Accordingly, Applicant submits that for at least this additional reason, Matsuura fails to teach each and every element of claim 45, as well.

With respect to claim 2, the Office Action states that current source 4a of Matsuura is "functionally equivalent" to the claimed current control transistor which controls a current flow through the amplifying transistor. Applicant disagrees. The claim specifically recites "current control transistor" as a structural element of the current path control section. Matsuura does not teach or suggest a current control transistor for providing a current to the amplifying transistor. Accordingly, for at least this additional reason, Applicant submits that Matsuura fails to teach each and every element recited in claim 2.

Therefore, Applicant requests that the rejection be reconsidered and withdrawn.

Conclusion

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222) at the telephone number of (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By _____

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